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ON-CHIP POWER-ON VOLTAGE INITIALIZATION

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CROSS-REFERENCE TO RELATED APPLICATION(S)

BACKGROUND

Field of the Invention

[1001] The present invention relates generally to integrated circuits and, more particularly, to initializing nodes of an integrated circuit.

Description of the Related Art

[1002] Typically, modern integrated circuits incorporate nodes e.g., latch nodes and memory nodes, that may power up in either of two states. These nodes preferably receive predetermined values upon applying power to the integrated circuit. The predetermined values are typically written during an initialization cycle. Writing predetermined values to a memory array generally consumes a significant amount of time, which increases with the size of the memory array. For example, the memory array may be initialized by executing a sequence of individual write instructions to the memory array. The initialization of memory arrays may increase test time of the memory design or delay commencing desired functional activity. Accordingly, there is a need for improved techniques for setting nodes of an integrated circuit to a predetermined value upon applying power to the integrated circuit.

SUMMARY

[1003] It has been discovered that initialization of a memory array can be improved by setting the nodes of the memory array to predetermined values automatically upon applying power to the integrated circuit. Data input nodes and a

memory write enable node are configured to store the predetermined values on the nodes of the memory array in response to successive enablement and automatic reset of word lines corresponding to the nodes of the memory array. Circuitry included for initializing control and data signals of the memory array is effectively disabled upon termination of the initialization. The integrated circuit may include circuitry that initiates and terminates the initialization, thus obviating an additional input/output pin for this purpose.

[1004] In some embodiments of the present invention, a method for initializing a memory circuit includes detecting that a power supply operably coupled to the memory circuit first achieves a first predetermined voltage. The method also includes asynchronously pulsing successive word line groups of one or more individual word lines of the memory array while conveying a data pattern onto bit lines of the memory array, to thereby write the data pattern into memory cells associated with each such word line group. The asynchronously pulsing may include, for at least one word line group, pulsing a first word line group in response to an input signal received from an earlier pulsed second word line group, generating an output signal delayed from the input signal, and conveying the delayed output signal to a third word line group.

[1005] In some embodiments of the present invention, a system includes an array of memory cells arranged in rows and columns, a plurality of word lines corresponding to respective rows of the array, a plurality of bit lines corresponding to respective columns of the array, and a plurality of serially-connected word line driver initialization circuits, each for pulsing a respective group of one or more individual word lines of the memory array. The system also includes a control circuit for generating an input signal for the first of the serially-connected word line driver initialization circuits when a power supply operably coupled to the memory circuit first achieves a first predetermined voltage. The system also includes a plurality of data circuits for conveying a data pattern onto the bit lines of the memory array during the pulsing of the word line groups. The system may include an initialization circuit including a first circuit, the first circuit being coupled to a first node and the power supply, the first circuit generating an enable signal having a response based at least in part on the power supply and the first predetermined voltage.

[1006] In some embodiments of the present invention, an integrated circuit includes a first node conveying an enable signal, a second node conveying an initialization signal, a level shifting circuit coupled to the first node and a power supply node, a hysteresis circuit coupled to the first and second nodes, and a latch node coupled to receive a first predetermined state in response to a first signal based at least in part on the initialization signal. The level shifting circuit generates the enable signal based at least in part on a signal conveyed by the power supply node and a predetermined initialization disable voltage. The hysteresis circuit generates the initialization signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[1007] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[1008] **FIG. 1** illustrates an exemplary system in accordance with some embodiments of the present invention.

[1009] **FIG. 2A** illustrates an exemplary word line driver initialization circuit in accordance with some embodiments of the present invention.

[1010] **FIG. 2B** illustrates an exemplary high pulse generator circuit in accordance with some embodiments of the present invention.

[1011] **FIG. 3A** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1012] **FIG. 3B** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1013] **FIG. 3C** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1014] **FIG. 3D** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1015] **FIG. 4** illustrates an exemplary voltage initialization circuit in accordance with some embodiments of the present invention.

[1016] **FIG. 5** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1017] **FIG. 6** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1018] **FIG. 7** illustrates exemplary signal waveforms in accordance with some embodiments of the present invention.

[1019] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[1020] A series of mechanisms have been developed for initializing nodes of an integrated circuit upon applying power to the integrated circuit. Referring to FIG. 1, memory array 102 is coupled to typical circuit elements 104, 106, 108, 110, 114, and 116. In addition, memory array 102 is coupled to initialization circuit elements 140, 142,..., 160, and 170. In an exemplary realization of the present invention, memory array 102 is an $M+1$ by $N+1$ bit static random access memory (SRAM) that, under typical operating conditions, is word line selectable, e.g., by signals driven by word line drivers 104, 106, and 108 on `WORD_LINE_0`, `WORD_LINE_1`,..., `WORD_LINE_M`. A word line may also be referred to as a row line or a select line and no inference to the organization of number of bits per word is implied by such terminology. The memory elements receive data from data latches 114 and 116 in response to the `WORD_LINE` signals and a write enable signal stored in write enable latch 110. Although only three such word lines are depicted, it should be understood that in actual practice many more word lines may be implemented. Similarly, while only two such data latches are depicted, it should be understood that in actual practice many more data latches may be implemented. Moreover, other critical signals, such as read control signals in the column circuitry, decoders, etc. may be implemented in actual practice.

[1021] Referring to the system 100 of FIG. 1 and corresponding waveforms in FIG. 3A, initialization is controlled by INIT, a signal generated on-chip by voltage initialization circuit 170. However, INIT may be generated off-chip and communicated to system 100 via an input/output port. In an exemplary system, INIT transitions low when the power supply node, during power-on transient, achieves a minimum functional voltage, i.e., a voltage at which the circuits of system 100 will function as intended. This functional voltage may be the same as or different from the operating voltage of the integrated circuit.

[1022] While INIT is high, discharge devices, e.g., n-type transistors 158 and 160 keep nodes within data latches, e.g., data latch bit_0 114 and data latch bit_N 116, so that the data latches power up with a known value of '0.' Note that this configuration will initialize the elements of memory array 102 to '0.' However, system 100 may be modified to initialize the elements of memory array 102 to '1' or to any combination of values by coupling the data latches to p-type transistors or a combination of n-type transistors and p-type transistors coupled to INIT and INIT_B. In addition, the initialization values may be programmable by selectively coupling (e.g., using fuses, anti-fuses, or any other suitable circuit element) data latches 114 and 116 to n-type transistors and p-type transistors according to a desired initialization pattern. INIT may be sufficiently buffered to drive any number of n-type transistors, p-type transistors or other devices that initialize signals coupled to memory array 102, or other memory circuits that are preferably initialized.

[1023] INIT_B enables pull-up device 152 to charge a node within write enable latch 110. During this time, INIT_DEL and INIT_PULSE_0, INIT_PULSE_1,...,INIT_PULSE_M are high and RST_0, RST_1,...,RST_M are low. Word line driver initialization circuits 140, 142, and 144 are effectively disabled, failing to charge or discharge WORD_LINE_0, WORD_LINE_1,...,WORD_LINE_M. When INIT transitions from high to low, transistors 152, 158, and 160 are turned off. However, assuming that clock signals to these latches are effectively disabled at this time, write enable latch 110 and data latches 114 and 116 hold the initialization values introduced by p-type transistor 152 and n-type transistors 158 and 160.

[1024] Upon a falling edge of INIT (i.e., when INIT transitions low), nand gate 150 and inverting delay 154 generate a low pulse on INIT_PULSE_0. Specifically, when INIT transitions low, INIT_B transitions high, and INIT_DEL remains high for an interval of time determined by the length of delay introduced by inverting delay 154. When both INIT_DEL and INIT_B are high, the output of nand 150, i.e., INIT_PULSE_0 is low. INIT_PULSE_0 remains low during an interval of time (i.e. during the width of the low pulse that is generated by inverting delay 154 and nand 150) that is a function of the length of the delay produced by inverting delay 154. In an exemplary embodiment, inverting delay 154 includes a series of inverters. However, nand gate 150 and inverting delay 154 are exemplary and may be substituted with any suitable circuits. When INIT is low, exemplary n-type transistors 158 and 160 are disabled and have no significant effect on data latches 114 and 116. INIT_B is high, and p-type transistor 152 is disabled, having no significant effect on write enable latch 110.

[1025] An exemplary word line driver initialization circuit 144 is illustrated in FIG. 2A. When INIT_PULSE_0 is high, p-type transistor 204 is effectively turned off. Upon a rising edge of INIT_PULSE_0, high pulse generator 202 generates a high pulse on RST_0. An exemplary high pulse generator circuit is illustrated in FIG. 2B, although high pulse generator 202 may be any suitable circuit. When INIT_PULSE_0 is high, RST_0 is low, effectively turning off n-type transistor 206. Since both p-type transistor 204 and n-type transistor 206 are effectively turned off when INIT_PULSE_0 is high, word line driver initialization circuit 144 fails to charge or discharge WORD_LINE_0, and WORD_LINE_0 and node 208 float if driver 128 is not driving WORD_LINE_0.

[1026] The falling transition of INIT causes inverting delay 154 and nand 150 of FIG. 1 to generate a low pulse on INIT_PULSE_0, as discussed above. Referring to FIG. 2A, this low pulse enables p-type transistor 204 of word line driver initialization circuit 144 to charge node 208 and WORD_LINE_0. Upon completion of the pulse on INIT_PULSE_0, i.e., INIT_PULSE_0 transitions high and high pulse generator 202 produces a high pulse on RST_0, consequently enabling n-type transistor 206. Then, n-type transistor 206 discharges node 208, effectively resetting

WORD_LINE_0. The high pulse generator 202 then drives node RST_0 back to ground, terminating the pulse, and disabling transistor 206.

[1027] Referring to FIGS. 1 and 3A, in some embodiments of the present invention, more than one word line is configured to be high to write corresponding memory elements during the interval that WORD_LINE_0 selects memory element(s) for initialization. The individual word lines may be pulsed in a partially or substantially overlapped group (see e.g., FIG. 3B and FIG. 3C), and may be uniformly deasserted (see e.g., FIG. 3D). However in an exemplary embodiment, driver circuits 140, 142, and 144 are configured to drive corresponding word lines during successive, non-overlapping intervals. For example, RST_0 is coupled to inverting delay 110 to generate INIT_PULSE_1. INIT_PULSE_1 is similar to INIT_PULSE_0, but is delayed, the amount of the delay determined by at least high pulse generator 202 and inverting delay 110. INIT_PULSE_1 enables a corresponding p-type transistor in word line driver initialization circuit 142 to drive WORD_LINE_1. INIT_PULSE_1 also drives a corresponding high pulse generator to produce RST_1, which resets the WORD_LINE_1. RST_1 triggers the initialization of the next word line in succession. Additional inverting delay circuits, e.g., inverting delay 146, may be coupled to successively enable multiple word lines for initialization of corresponding memory elements included in memory array 102 or other memory elements on the integrated circuit. In some realizations of the present invention, the word lines are successively enabled asynchronously (i.e., without reference to a timing clock) within a single clock cycle. This may be achieved for a sufficiently large number of word lines by operating at a slow clock speed during initialization, or by any other suitable technique.

[1028] During post-initialization operation, INIT is low, i.e., '0', and initialization circuit elements 140, 142, ..., 160 are effectively disabled, e.g., circuit elements 140, 142, ..., 160, and 170 do not drive word lines and latches coupled to these circuit elements. For example, when INIT is '0', discharge devices 158 and 160 are effectively disabled, thus failing to discharge or otherwise interfere with operation of data latch bit 0 and data latch bit N. Under these circumstances, INIT_B is high, i.e., '1', and pull-up transistor 152 is effectively disabled, thus failing to charge or otherwise interfere with operation of write enable latch 110. In addition, word line

driver initialization circuits 140-44 are effectively disabled, i.e., word line driver initialization circuits 140, 142, and 144 fail to drive WORD_LINE_0, WORD_LINE_1,..., WORD_LINE_M. Signals from drivers 104, 106, and 108 and clocked signals or other signals driven to write enable latch 110 and data latches 114 and 116 will not be substantially impeded by the initialization circuitry during post-initialization operation.

[1029] Although INIT may be received from an input/output pin, this signal may be generated on-chip by voltage initialization circuit 170. An exemplary voltage initialization circuit 170 is illustrated in FIG. 4. Voltage initialization circuit 170 is coupled to initialize a single illustrative latch 430. When INIT is high, transistors 420 and 428 are effectively enabled and node 424 is charged or discharged according to selective connectors 422 and 426, respectively. Typically, only one of n-type transistor 428 and p-type transistor 420 may be present or may be effectively coupled to node 424 for a given latch. Selective connectors 420 and 426 may be fuses, anti-fuses, or any other suitable device. When INIT is low, n-type transistor 428 and p-type transistor 420 are effectively disabled and node 424 receives data according to the clock signal.

[1030] On-chip voltage initialization circuit 170 includes circuitry to generate an INIT signal consistent with system 100 and consistent with initializing node 424 of circuit 400, and other similar systems. On-chip voltage initialization circuit 170 includes a level shifting circuit, i.e., a number of p-type transistors with grounded gate terminals, e.g., p-type transistors 402 and 410, coupled in series and coupled to weak n-type transistors (i.e., an n-type transistor designed to have a low gain achieved by a small W/L ratio) with gate terminals coupled to a power supply node, e.g., n-type transistors 404 and 412, respectively. The output of these p-type transistors, e.g., node 414, is coupled to a Schmitt trigger, e.g., circuit 416. The power supply transitions slowly from 0V to an operating voltage, e.g., 1.3 V. At the start of this transition, the voltage across the gate and source of p-type transistor 402 and the voltage across the gate and source of p-type transistor 410 are below the threshold voltage of these p-type transistors. Once the power supply voltage reaches the threshold voltage and continues to slowly increase, p-type transistors 402 and 410 begin to slowly draw current. While these currents are small, the weak n-type

transistors 404 and 412 maintain a low voltage at nodes 406 and 414, respectively. Weak p-type transistor 418 (i.e., a p-type transistor designed to have a low gain achieved by a small W/L ratio) maintains INIT at the supply voltage until circuit 416 resets, i.e., transitions to '0'.

[1031] Once the power supply reaches a sufficient voltage level (e.g., 100mV in 130nm technology) above the p-type transistor threshold voltage, p-type transistor 402 begins to overcome the weak n-type transistor 404. A short time later, p-type transistor 410 wins over weak n-type transistor 412 and node 414 begins to transition high. Once node 414 reaches the threshold voltage of Schmitt trigger 16, the output of circuit 416 transitions low, i.e., circuit 416 overcomes weak p-transistor 418 and the INIT node transitions to 0V. This behavior is illustrated in FIGS. 5 and 6. Circuit block 408 may be repeated and coupled according to a desired power supply voltage that disables the INIT signal since each such stage 408 increases the effective trip point of 416 by about 50mV for an exemplary embodiment. INIT drives a device that initializes a node of memory element 430. For example, the node of memory element 430 may be p-type transistor 420 or n-type transistor 428 selectably coupled to node 424, or another n-type or p-type transistor coupled to node 424.

[1032] Circuit 416 is typically a Schmitt trigger circuit, i.e., a circuit that responds to a slowly changing input waveform with fast transition times at the outputs and which includes different input thresholds for rising and falling input voltage signals. Circuit 416 has a threshold voltage for the rising input signal that is higher than the threshold voltage for the falling input signal, i.e., the input voltage that an input signal must fall below to transition the output to a high voltage is lower than the input voltage that an input signal must exceed to transition the output to a low voltage. An exemplary embodiment of a Schmitt trigger circuit is illustrated in FIG. 4, but any Schmitt trigger circuit or other suitable hysteresis circuit may be substituted for circuit 416. The hysteresis characteristic of circuit 416 provides tolerance to noisy signals. Once the power supply reaches a functional voltage, INIT remains low although substantial noise glitches occur on the power supply. This characteristic is illustrated in FIG. 7. Although a 100mV glitch occurs on the power supply, the INIT signal remains off.

[1033] While circuits and physical structures are generally presumed, it is well recognized that in modern semiconductor design and fabrication, physical structures and circuits may be embodied in computer readable descriptive form suitable for use in subsequent design, test, or fabrication stages as well as in resultant fabricated semiconductor integrated circuits. Accordingly, claims directed to traditional circuits or structures may, consistent with particular language thereof, read upon computer readable encodings and representations of same, whether embodied in media or combined with suitable reader facilities to allow fabrication, test, or design refinement of the corresponding circuits and/or structures. In addition, structures and functionality presented as discrete components in the exemplary configurations may be implemented as a combined structure or component. Finally, various features of certain embodiments of the present invention may be used alone or in combination. These and other variations, modifications, additions, and improvements may fall within the scope of the invention as defined in the claims that follow.